We Claim:

1. A method for producing a vertical transistor having a gate electrode, a gate oxide, an upper source/drain region, and a lower source/drain region, the method which comprises:

producing at least one first trench in a substrate;

producing a sacrificial gate oxide on at least a first trench wall;

producing a sacrificial gate electrode on the sacrificial gate oxide;

producing an insulation structure for insulation between different vertical transistors;

removing the sacrificial gate electrode from the trench;

removing the sacrificial gate oxide from the trench;

at least at a location of the sacrificial gate oxide, producing the gate oxide on the trench wall;

producing the gate electrode on the gate oxide; and

producing the upper source/drain region and the lower source/drain region.

2. The method according to claim 1, wherein the step of removing the sacrificial gate oxide is carried out by an isotropic etching.

3. The method according to claim 1, wherein the step of removing the sacrificial gate oxide is carried out by a wet-chemical etching.

4. The method according to claim 1, which comprises using trench insulation as the insulation structure.

5. The method according to claim 4, which comprises:

producing at least one second trench for generating the trench insulation; and

filling the second trench with an insulating material such that a first trench insulation wall forms an edge with the first trench wall.

6. The method according to claim 5, which comprises, during the step of removing the sacrificial gate oxide, removing the insulating material from the trench insulation in a region of

the first trench insulation wall such that at least one substrate edge is exposed.

7. The method according to claim 6, wherein the gate oxide is also applied to the substrate edge.

8. The method according to claim 6, which comprises forming a gate electrode having an internal angle α of 90° or less with the first trench insulation wall.

9. The method according to claim 1, which comprises, before performing the step of producing the sacrificial gate oxide, producing an insulation layer on a base of the first trench.

10. The method according to claim 9, wherein the insulation layer is a silicon nitride layer.

11. The method according to claim 1, which comprises performing at least one step selected from a group consisting of the step of producing the sacrificial gate oxide and the step of producing the gate oxide by a thermal oxidation.

12. The method according to claim 1, wherein the insulating structure includes an insulating material produced from silicon dioxide.

13. The method according to claim 1, which comprises using polysilicon as a material of at least one electrode selected from a group consisting of the sacrificial gate electrode and the gate electrode.

14. The method according to claim 1, wherein the vertical transistor is produced over an energy storage capacitor and forms a part of a memory cell.

15. The method according to claim 1, wherein the vertical transistor forms a part of a DRAM memory cell.

16. A vertical transistor, comprising:

at least one trench wall;

a plurality of source/drain regions;

a channel region running essentially vertically on said trench wall;

a gate electrode;

a gate oxide insulating said gate electrode from said channel region; and

at least one insulation structure for insulating between different vertical transistors;

said insulation structure bounding said gate electrode; and

said gate electrode having an internal angle α of 90° or less with said insulation structure.

17. The vertical transistor according to claim 16, wherein said insulation structure is trench insulation.

18. The vertical transistor according to claim 16, comprising:

an essentially vertical substrate edge;

said insulation structure bounding said gate electrode in a region in which said gate oxide covers said essentially vertical substrate edge.

19. The vertical transistor according to claim 16, comprising:

an essentially vertical substrate edge;

said insulation structure being trench insulation; and

said gate electrode at least partially covering said gate oxide in a region of said essentially vertical substrate edge.

20. The vertical transistor according to claim 16, wherein said gate electrode forms an internal angle α of 60° or less with said insulation structure.

21. The vertical transistor according to claim 16, in combination with a memory cell, wherein said memory cell includes an energy storage capacitor and said vertical transistor is formed above said storage capacitor.